

BWD4426-1

Dual Inverting MOSFET Driver Die

DUAL CHANNEL / 1.5 A PEAK OUTPUT / BARE DIE

Issued 2019-08-02 | Effective 2019-08-14

General Description

The BWD4426-1 is a high-reliability, dual-channel MOSFET driver fabricated using a BCDMOS process for low power consumption and high efficiency. It translates TTL/CMOS logic inputs into high- and low-level outputs that swing to within 25 mV of the supply rails under no-load conditions. The BWD4426-1 provides two inverting channels.

Features

- Bipolar/CMOS/DMOS process
- 1.5 A peak output current
- Latch-up protection: >500 mA reverse current
- 4.5 V to 18 V operating supply
- Supply current: 4 mA (logic high); 400 μ A (logic low)
- Switches a 1000 pF load in 25 ns
- 7 Ω typical output impedance
- Typical propagation delay <40 ns
- TTL/CMOS-compatible inputs

Applications

Power MOSFET drive; low-impedance capacitive, resistive and inductive loads requiring high peak current and fast switching; clock lines; coaxial cables; piezoelectric transducers.

Functional Block Diagram

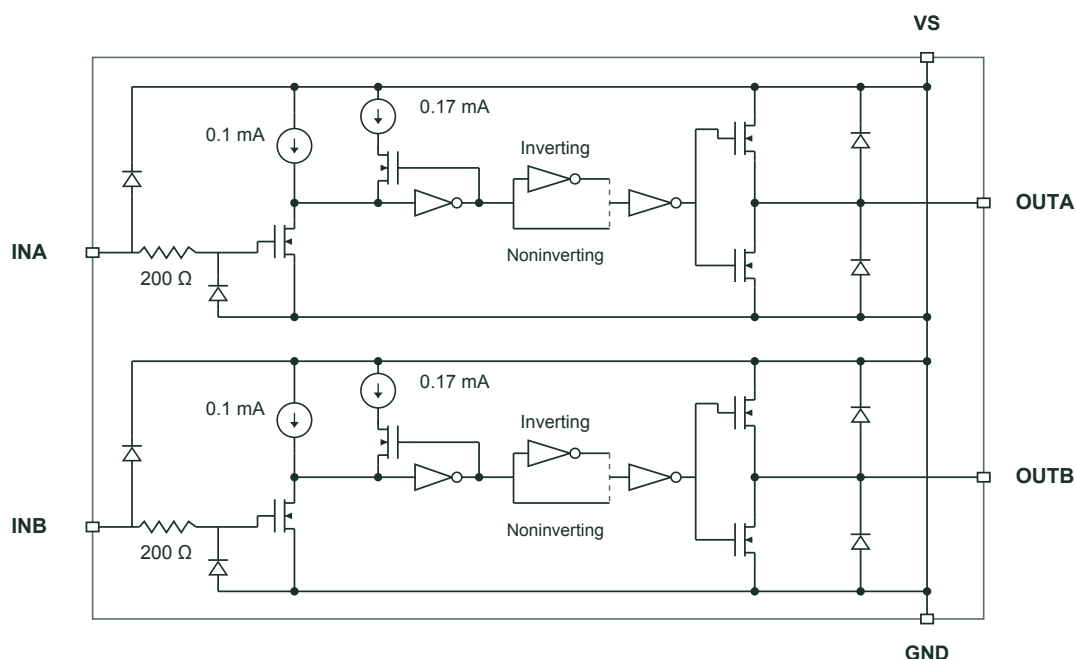


Figure 1. Functional block diagram.

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Electrical Specifications

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply voltage	22	V
Input voltage	GND - 0.3 to $V_S + 0.3$	V

Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply voltage	4.5	18	V
Logic-high input voltage, V_{IH}	2.4	-	V
Logic-low input voltage, V_{IL}	-	0.8	V

Electrical Characteristics

Unless otherwise specified: $4.5\text{ V} \leq V_S \leq 18\text{ V}$. A dash indicates an unspecified value.

Parameter	Conditions	Min	Typ	Max	Unit
Output high voltage	-	$V_S - 0.025$	-	-	V
Output low voltage	-	-	-	0.025	V
Input leakage current	$0 \leq V_{IN} \leq V_S$	-1	-	1	μA
High-state output resistance	$V_S = 18\text{ V}; I_{OUT} = -10\text{ mA}$	-	6	10	Ω
Low-state output resistance	$V_S = 18\text{ V}; I_{OUT} = 10\text{ mA}$	-	6	10	Ω
Peak output current	-	-	1.5	-	A
Quiescent supply current	$V_{INA} = V_{INB} = 3\text{ V}$	0.6	1.4	4.5	mA
Quiescent supply current	$V_{INA} = V_{INB} = 0\text{ V}$	-	0.18	0.4	mA

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Performance Characteristics

Supply Voltage and Frequency

FIGURE 02

Rise / fall time vs. supply voltage

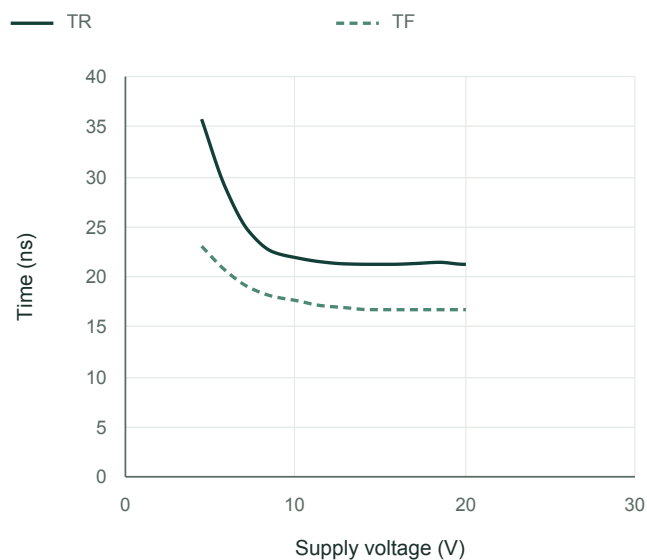


FIGURE 03

Propagation delay vs. supply voltage

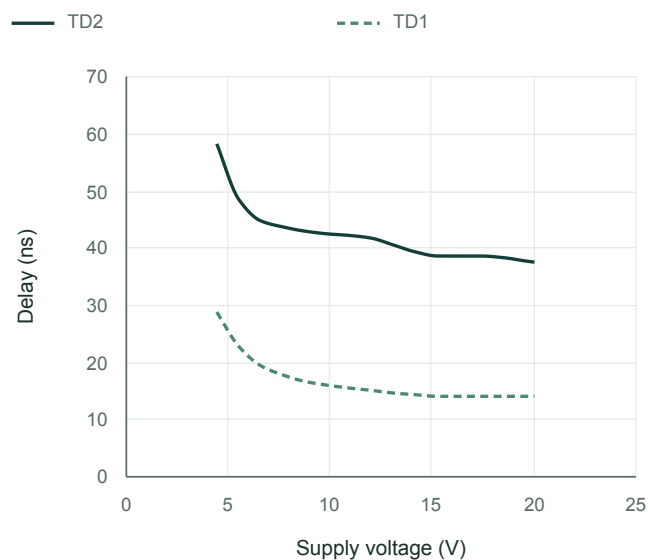
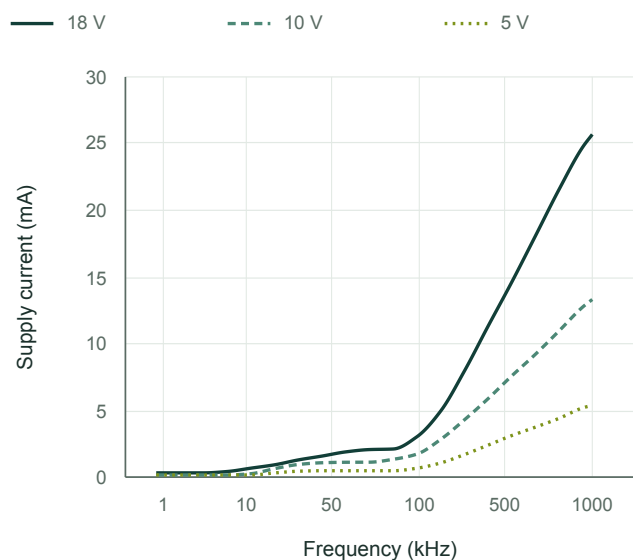


FIGURE 04

Supply current vs. frequency



Reading the curves

Performance curves illustrate characteristic trends. Use the electrical-characteristics tables for specified Min / Typ / Max values and test conditions.

The curves have been digitized from the supplied plots. Values are approximate; axis ranges and labeled tick positions follow those plots.

Note: Curves are digitized from the supplied characterization plots and are approximate. They do not establish additional guaranteed limits.

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Performance Characteristics (Continued)

Output Characteristics and Supply Current

FIGURE 05

High-state voltage drop vs. load current

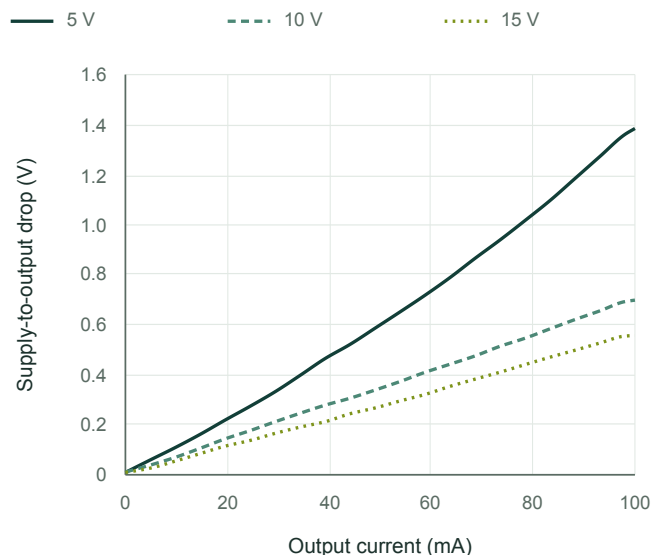


FIGURE 06

Low-state output voltage vs. load current

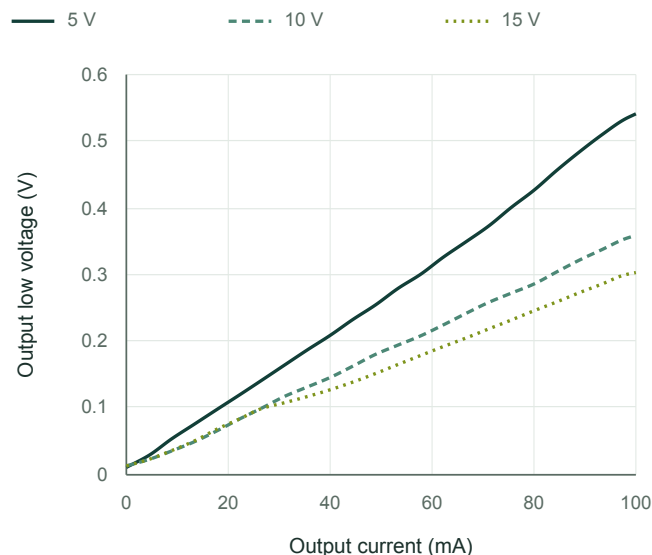


FIGURE 07

Quiescent current vs. supply voltage

Logic-high input

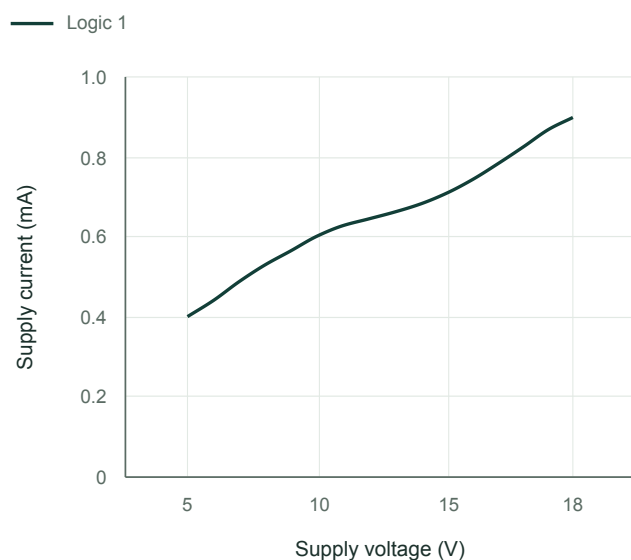
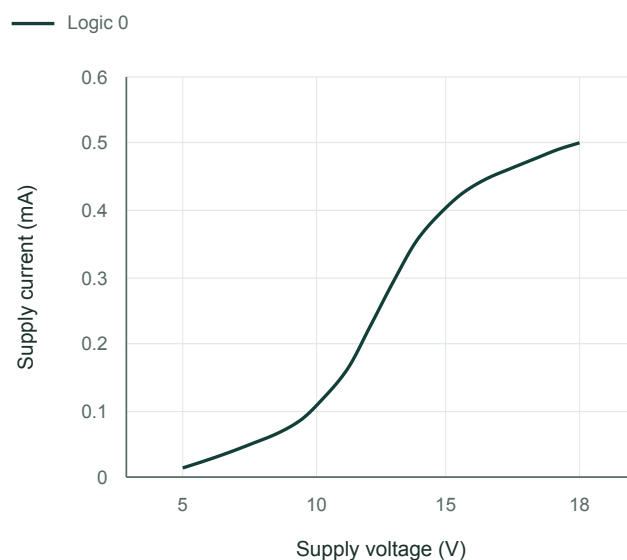


FIGURE 08

Quiescent current vs. supply voltage

Logic-low input



Note: Curves are digitized from the supplied characterization plots and are approximate. They do not establish additional guaranteed limits.

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Performance Characteristics (Continued)

Capacitive Load and Temperature

FIGURE 09

Dynamic current vs. load capacitance

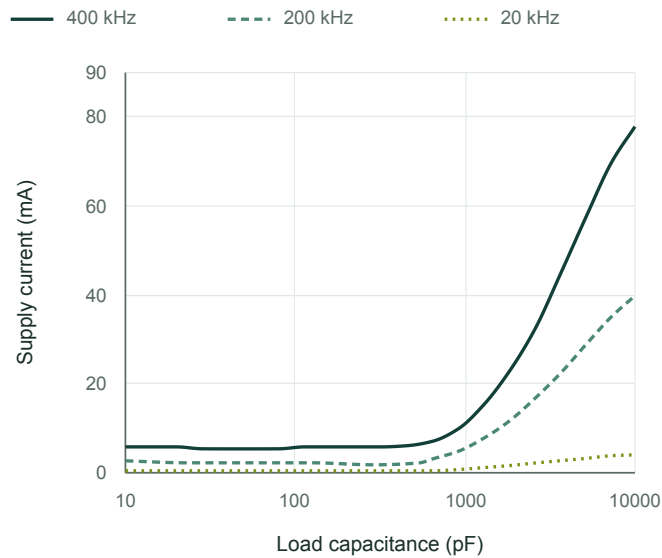


FIGURE 10

Rise / fall time vs. load capacitance

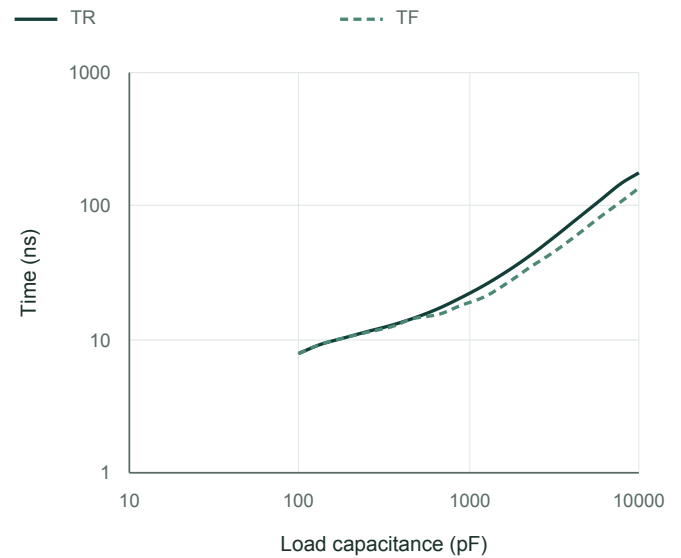


FIGURE 11

Propagation delay vs. temperature

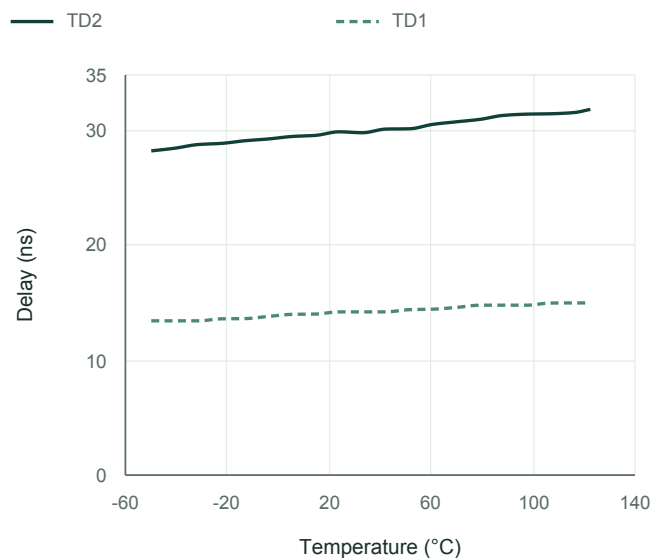
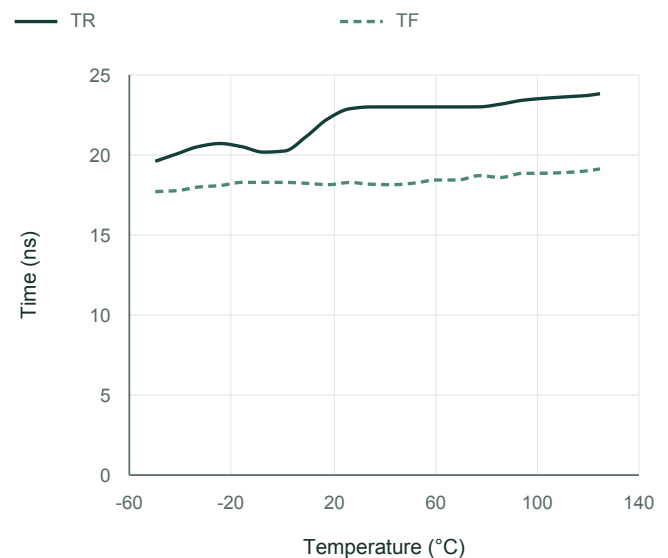


FIGURE 12

Rise / fall time vs. temperature



Note: Curves are digitized from the supplied characterization plots and are approximate. They do not establish additional guaranteed limits.

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Switching Characteristics and Application

Switching Characteristics

Parameter / symbol	Conditions	Min	Typ	Max	Unit
Minimum pulse width, T_{PW}	See test circuit below	400	-	-	ns
Output rise time, T_R	-	-	18	30	ns
Output fall time, T_F	-	-	15	20	ns
Propagation delay, T_{D1}	-	-	17	30	ns
Propagation delay, T_{D2}	-	-	23	50	ns

Typical Application / Switching-Time Test Circuit

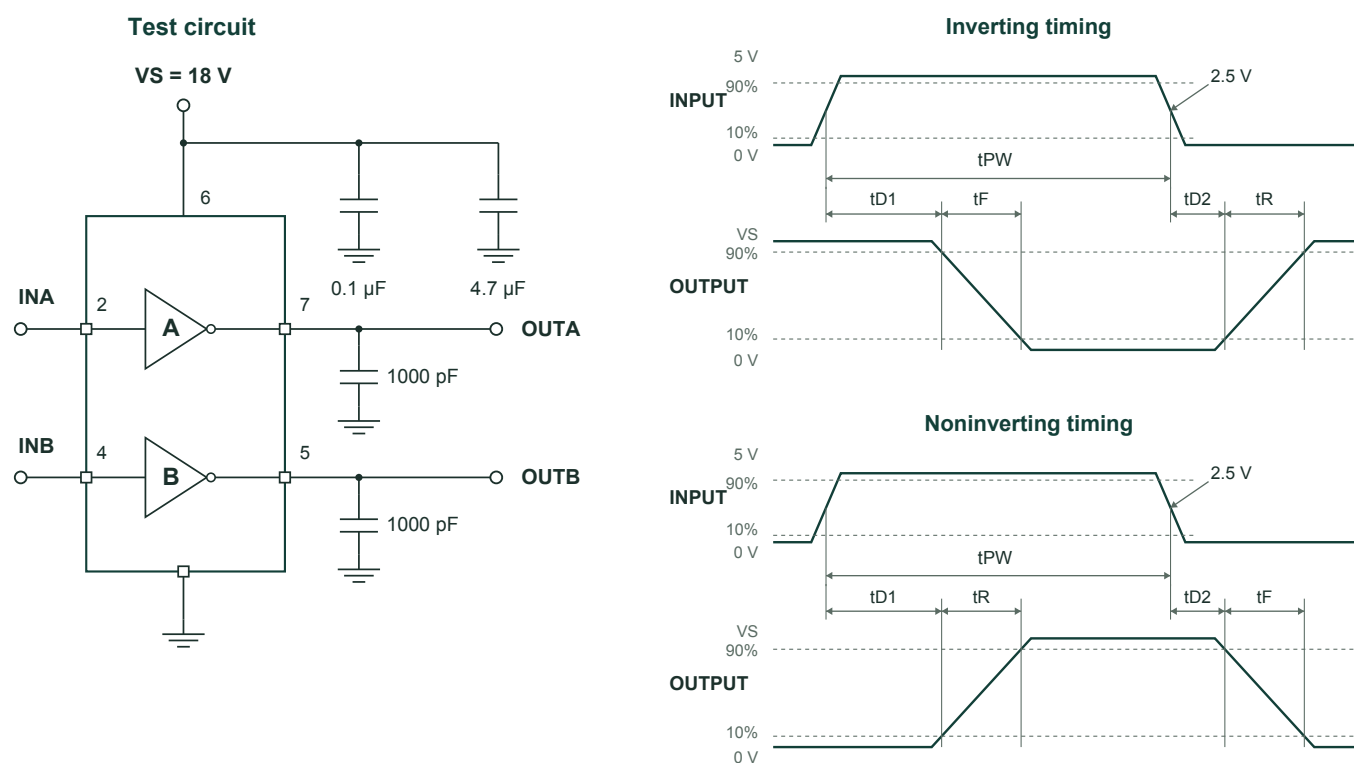


Figure 13. Test circuit and timing diagrams. $V_S = 18\text{ V}$, $C_L = 1000\text{ pF}$ per output; supply bypass capacitors are $0.1\text{ }\mu\text{F}$ and $4.7\text{ }\mu\text{F}$.

Both inverting and noninverting timing diagrams are shown. The BWD4426-1 is a dual inverting device. Circuit pin numbers differ from the bare-die pad numbers on the following page.

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Bare-Die Information and Bond Pads

Die Information

Die information	Specification
Top metallization	Al
Backside material	Si
Backside electrode	Floating
Die size (L × W)	55 × 51 mils
Die thickness	Not specified
Die drawing number	H001284
Recommended storage	High-purity nitrogen

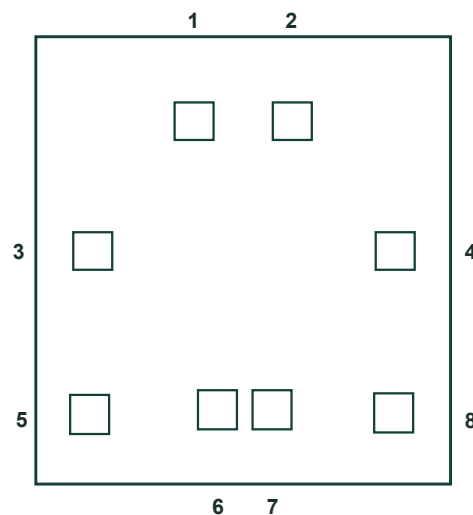


Figure 14. Bond-pad layout.

Bond-Pad Coordinates

Pad	Name / function	X (μm)	Y (μm)
1	VDD	485	1022
2	VDD	728	1022
3	OUTA (inverting)	153	612
4	OUTB (inverting)	1058	612
5	INA	135	150
6	GND	540	150
7	GND	668	150
8	INB	1075	150

Application Notes

Validate the device in the intended application under the stated supply, load and operating conditions. Typical performance curves illustrate device behavior and do not establish additional guaranteed limits.